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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,741	12/29/2003	Takahisa Ueno	075834.00457	2068
33448	7590	05/27/2010	EXAMINER	
ROBERT J. DEPK	LEWIS T. STEADMAN		NGUYEN, LUONG TRUNG	
ROCKEY, DEPK & LYONS, LLC	SUITE 5450 SEARS TOWER		ART UNIT	PAPER NUMBER
CHICAGO, IL 60606-6306			2622	
			MAIL DATE	DELIVERY MODE
			05/27/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/747,741	Applicant(s) UENO ET AL.
	Examiner LUONG T. NGUYEN	Art Unit 2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 17 May 2010.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 16-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 16-23 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____
- 5) Notice of Informal Patent Application
 6) Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/17/2010 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 16-23 filed on 05/17/2010 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 16-18, 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda et al. (US 5,898,168) in view of Tanaka et al. (US 6,674,470) further in view of Hamasaki (US 5,187,583).

Regarding claim 16, Gowda et al. discloses a solid state imaging element (imager 20, figures 3A-3B) comprising:

a pixel (cell 30; figures 3A-3B; column 4, lines 9+) to which has a photoelectric transfer element (photodiode 26, figure 3B, column 4, lines 9-20), a transfer switch (FET 22, figure 3B, column 4, lines 9-36) for transferring charge stored in said photoelectric transfer element, a charge store part (circuit node 25, figure 3B, column 4, lines 37-62) for storing charge transferred by said transfer switch, a reset switch (reset transistor 21, figure 3B, column 4, lines 20-62) for resetting said charge store part, and an amplifying element (FET 23, figure 3B, column 4, lines 9-36) for outputting signal in accordance with the potential of said charge store part to vertical signal lines (column buses 15j, figures 3A-3B, column 4, lines 9-62).

Gowda et al. fails to specifically disclose wherein a threshold voltage of said amplifying element is reduced in relation to remaining transistors of each pixel. However, Tanaka et al. teaches an image sensor, in which the amplifying transistor has a low threshold voltage, this indicates that the threshold voltage of the amplifying is reduced (column 16, lines 50-55); and noted that each unit cell (pixel) in Figure 7 includes other transistors such as reset transistor 96, read-out transistors 93a, 93b in addition to amplifying transistor 94; all these transistors are connected each other (i.e., relation to each other); this indicates that the threshold voltage of the amplifying 94 is reduced in relation to reset transistor 96, read-out transistors 93a, 93b (column 16, lines 30-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Gowda et al. by the teaching of Tanaka et al. in

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order to obtain a solid state imaging device which have a wide amplifying function (column 16, lines 50-52).

Gowda et al. and Tanaka et al. fail to disclose wherein a diffusion region that is connected to a power source is laid out to be physically adjacent to the photoelectric conversion element in order to provide an overflow path. However, Hamasaki discloses a solid state imager which comprises a floating diffusion (FD) connected to power supply voltage VDD and is adjacent to a photodiode (figures 1-2, column 3, lines 8-19; column 5, line 58 – column 6, line 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Gowda et al. and Tanaka et al. by the teaching of Hamasaki in order to provide an overflow train (column 5, line 58 - column 6, line 8).

Regarding claim 17, Gowda et al. discloses wherein said transfer switch is an enhancement type transistor (FET 22, figure 3B, column 4, lines 9-36).

Regarding claim 18, Gowda et al. discloses wherein said amplifier is an enhancement type transistor (FET 23, figure 3B, column 4, lines 9-36).

Regarding claims 20-22, Tanaka et al. discloses wherein the amplifying element operates linearly across its entire range of operation (Tanaka et al. discloses an image sensor, in which the

amplifying transistor has a low threshold voltage, this indicates that the threshold voltage of the amplifying can be reduced and can be linearly operated, column 16, lines 50-55).

5. Claims 19, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al. (US 5,886,659) in view of Tanaka et al. (US 6,674,470) further in view of Hamasaki (US 5,187,583).

Regarding claim 19, Pain et al. discloses a solid state imaging element (figures 1A-1C, 3A, 4; column 3, lines 55+; column 6, lines 10+) comprising:

a pixel (pixel in pixel array 410; figure 4; column 6, lines 50+) to which has a photoelectric transfer element (figures 2A, 3A; photodiode 210, photogate 310; column 6, lines 14-33), a transfer switch (transfer gate electrode 320, figure 3A; column 6, lines 25+) for transferring charge stored in said photoelectric transfer element, a charge store part (floating diffusion 330, figure 3A; column 6, lines 25+) for storing charge transferred by said transfer switch, a reset switch (reset electrode 340; figure 3A; column 9, lines 25+) for resetting said charge store part, and an amplifying element (transistor 360, figure 3A; column 3; lines 55-60) for outputting signal in accordance with the potential of said charge store part to vertical signal lines (figures 3A, 4; column 6; lines 24+);

wherein negative voltage is applied to the gate of said reset switch (column 6, lines 40-43).

Pain et al. fails to specifically disclose wherein a threshold voltage of said amplifying element is reduced in relation to remaining transistors of each pixel. However, Tanaka et al.

teaches an image sensor, in which the amplifying transistor has a low threshold voltage, this indicates that the threshold voltage of the amplifying is reduced (column 16, lines 50-55); and noted that each unit cell (pixel) in Figure 7 includes other transistors such as reset transistor 96, read-out transistors 93a, 93b in addition to amplifying transistor 94; all these transistors are connected each other (i.e., relation to each other); this indicates that the threshold voltage of the amplifying 94 is reduced in relation to reset transistor 96, read-out transistors 93a, 93b (column 16, lines 30-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Pain et al. by the teaching of Tanaka et al. in order to obtain a solid state imaging device which have a wide amplifying function (column 16, lines 50-52).

Pain et al. and Tanaka et al. fail to disclose wherein a diffusion region that is connected to a power source is laid out to be physically adjacent to the photoelectric conversion element in order to provide an overflow path. However, Hamasaki discloses a solid state imager which comprises a floating diffusion (FD) connected to power supply voltage VDD and is adjacent to a photodiode (figures 1-2, column 3, lines 8-19; column 5, line 58 – column 6, line 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Pain et al. and Tanaka et al. by the teaching of Hamasaki in order to provide an overflow train (column 5, line 58 - column 6, line 8).

Regarding claim 23, Tanaka et al. discloses wherein the amplifying element operates linearly across its entire range of operation (Tanaka et al. discloses an image sensor, in which the amplifying transistor has a low threshold voltage, this indicates that the threshold voltage of the amplifying can be reduced and can be linearly operated, column 16, lines 50-55).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LUONG T NGUYEN/
Primary Examiner, Art Unit 2622
05/24/10